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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,160	06/27/2001	Gerald Friese	00 P 7563 US 01 (8055-83	4594
48154	7590	12/19/2005	EXAMINER	
SLATER & MATSIL LLP 17950 PRESTON ROAD SUITE 1000 DALLAS, TX 75252			SONG, MATTHEW J	
			ART UNIT	PAPER NUMBER
			1722	

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 09/893,160	<b>Applicant(s)</b> FRIESE, GERALD	
	<b>Examiner</b> Matthew J. Song	<b>Art Unit</b> 1722	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 19 August 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-8 and 10-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 10-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)                                    | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 6-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al (US 6,159,826).

Kim et al discloses a conductive, metal line **52a** of an internal circuit (col 2, ln 5-10 and col 3, ln 35-36), this reads on applicant's metal layer. Kim et al also discloses a conductive region **55** fills a via hole formed in a first insulating layer **53**, where the first insulating layer reads on applicant's dielectric and the conductive region reads on applicant's interconnect. Kim et al also discloses a bond pad **56** having a first portion **56** disposed over the metal layer and the interconnect, and a second portion of **56** disposed over the dielectric layer, which is offset from the metal line (col 3, ln 45-55 and Fig 5 and 9). The portion of **56**, which does not overlie the metal line **52a**, reads on applicant's probe area. Kim et al also discloses a first portion including a bond pad **36** for providing an attachment point for a connection (col 1, ln 20-35). Kim et al also discloses a second insulating layer **57**, this reads on applicant's passivation layer, from on the first insulating layer **53** and the first portion **56a** and the second portion **56b** are exposed out the second insulating layer, this reads on applicant's passivation layer includes a first opening and a

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second opening. Figure 9 depicts the chip after dicing, which includes the bond pad and the portion of the bond, which overlies the insulating layer and is offset from the metal line.

Referring to claim 1, Kim et al discloses a bond pad area 56 and an insulating layer 53 (Fig 9), this reads on applicant's bond area is separated from the probe area. Kim et al also discloses a portion of 56 does not overlie the metal line 52a and overlies an insulating layer 53 (Fig 9), this reads on applicant's second portion is disposed over the dielectric layer and offset from the metal line. Furthermore, the portion of layer 56, which does not overlie the metal line 52a (Figs 5-6 and 9) reads on applicant's probe pad disposed over a dielectric and offset from a metal line because a bond pad can also function as a probe pad, as evidenced by page 3 of the instant specification.

Referring to claim 8, Kim et al discloses a separate probe area and bond area. However, the bond area can inherently be used as a probe area, note page 3 of the instant specification; therefore the bond area opening inherently includes a probe area.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826).

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Kim et al discloses all of the limitations of claim 24, as discussed previously, except a bond wire attached to the bond pad

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al by attaching a bond wire to the bond pad because the bond pad's is to provide a connection a bond wire.

Claims 3, 4, 10, 12, 15, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826) in view of Yoshioka (US 5,357,136).

Kim et al discloses all of the limitations of claim 4, as discussed previously, except a barrier layer disposed between the interconnect and the metal layer to prevent diffusion therebetween.

In a method of making a semiconductor device with a bond pad region, note entire reference, Yoshioka teaches a metal layer 15 formed of a refractory metal (col 4, ln 45-50), an interconnect 19 formed through a oxide insulator, which may contain phosphorus or boron 14 connecting to the metal layer (col 4, ln 55-60), and a bond pad 30 (col 4, ln 15-25 and col 5, ln 20-25). Yoshioka also teaches the barrier metal layer may consist of TiN, TiW, or W (col 4, ln 1-10). Yoshioka also teaches a barrier metal layer serves to prevent solid phase epitaxy in the opening of an integrated circuit device employing a conductive pattern (col 1, ln 30-40). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al by employing the barrier metal layer taught by Yoshioka to prevent solid phase epitaxy ('136 col 1, ln 30-40).

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826) as applied to claim 1 above, and further in view of Cheung et al (US 5,785,236) or Zawaideh (US 5,877,557).

Kim et al teaches all of the limitations of claim 1, as discussed previously, except the bond pad include aluminum.

In a method of wire bonding for integrated circuits, note entire reference, Cheung et al teaches a metal interconnect formed over an integrated circuit structure, forming an aluminum pad over the metal interconnect and bonding a metal wire to the aluminum pad (col 2, ln 50 to col 3, ln 5). Cheung et al also teaches a layer of conventional aluminum is patterned to form at least one aluminum pad (col 3, ln 40-55). Cheung et al also teaches an insulating layer or passivating layer is formed on the aluminum pad and patterned to expose the surface of the pad (col 3, ln 56-67). Cheung et al also teaches wire bonding to the pad (col 4, ln 10-25). Cheung et al also teaches bonding pad openings are formed in a passivation layer (col 3, ln 60-67). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al by using the aluminum pad taught by Cheung et al because the selection of a known material based on its suitability for its intended use is held to be obvious (MPEP 2144.07).

In a method of making a semiconductor device, note entire reference, Zawaideh teaches aluminum is often used as a conductive metal in semiconductor devices (col 1, ln 10-15) and aluminum is used in integrated circuits to form aluminum plugs, aluminum interconnects, aluminum bonding pads and other such structures (col 2, ln 15-20). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al by using

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the aluminum pad taught by Zawaideh because the selection of a known material based on its suitability for its intended use is held to be obvious (MPEP 2144.07).

6. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826) as applied to claim 1 above, and further in view of Wood et al (US 6,107,122).

Kim et al teaches all of the limitations of claim 5, as discussed previously, except the bond pad has a thickness of less than 2 microns.

In a method of making a semiconductor device, note entire reference, Wood et al teaches typical aluminum bond pads having a thickness of from 1.0 to 1.5  $\mu\text{m}$  (col 5, ln 25-26). Wood et al also teaches electrodes can comprise thin film aluminum bond pads in electrical communication with integrated circuits (col 5, ln 15-30). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al by using the aluminum pad with a thickness of 1.0 to 1.5  $\mu\text{m}$  taught by Wood et al because the thickness is conventionally used in the art for bonding pads.

Referring to claim 5, the combination of Kim et al and Wood et al teaches a bond pad thickness of 1.0-1.5  $\mu\text{m}$ . Overlapping ranges are held to be obvious (MPEP 2144.05).

7. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826) as applied to claim 1 above, and further in view of Admission (Applicant's admitted prior art).

Kim et al teaches all of the limitations of claim 2, as discussed previously, except the metal layer includes copper.

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In applicant's admitted prior art, Admission teaches copper metallizations are employed due to their high conductivities and aluminum is used as cap. Admission also teaches copper metallization for metal lines and an aluminum bond pad. Admission also teaches a diffusion barrier, which may include Ta or TaN is deposited between the copper and aluminum to prevent diffusion therebetween (page 1-3 of the instant specification).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al by using a copper metal layer and an aluminum bond pad because the selection of a known material based on its suitability for its intended use is held to be obvious (MPEP 2144.07).

Referring to claim 4, Kim et al does not teach a diffusion barrier. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al with Admission diffusion barrier to prevent diffusion between copper and aluminum, which is detrimental to resistivity (page 2 of Admission).

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826) as applied to claim 1 above, and further in view of Cain (US 5,656,945).

Kim et al teaches all of the limitations of claim 9, as discussed previously, except the bond pad is permanently connected to a bond wire.

In a method of testing electrical device, Cain teaches mounting a die within a package typically involves attaching a die with a socket formed in the package and permanently attaching package leads to the wire bond pads, by wire bonding, lead bonding or soldering, this reads on applicant's bond pad is permanently connected to a bond wire (col 2, ln 1-25). It would have



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been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al by permanently connecting a package lead to a bond pad to form a package, which can be tested (col 1, ln 45-67).

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826) in view of Yoshioka (US 5,357,136) as applied to claim 10 above, and further in view of Wood et al (US 6,107,122).

The combination of Kim et al and Yoshioka teaches all of the limitations of claim 14, as discussed previously, except the bond pad with a thickness of less than about 2 microns.

In a method of making a semiconductor device, note entire reference, Wood et al teaches typical aluminum bond pads having a thickness of from 1.0 to 1.5  $\mu\text{m}$  (col 5, ln 25-26). Wood et al also teaches electrodes can comprise thin film aluminum bond pads in electrical communication with integrated circuits (col 5, ln 15-30). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Kim et al and Yoshioka by using the aluminum pad with a thickness of 1.0 to 1.5  $\mu\text{m}$  taught by Wood et al because the thickness is conventionally used in the art for bonding pads.

Referring to claim 5, the combination of Kim et al, Yoshioka and Wood et al teaches a bond pad thickness of 1.0-1.5  $\mu\text{m}$ . Overlapping ranges are held to be obvious (MPEP 2144.05).

10. Claims 11-13, 18-19, and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826) in view of Yoshioka (US 5,357,136) as applied to claim 10 above, and further in view of Admission (Applicant's admitted prior art).

The combination of Kim et al and Yoshioka teaches all of the limitations of claim 11, as discussed previously, except the metal layer includes copper.

In applicant's admitted prior art, Admission teaches copper metallizations are employed due to their high conductivities and aluminum is used as cap. Admission also teaches copper metallization for metal lines and an aluminum bond pad. Admission also teaches a diffusion barrier, which may include Ta or TaN is deposited between the copper and aluminum to prevent diffusion therebetween (page 1-3 of the instant specification).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al or Yoshioka by using a copper metal layer and an aluminum bond pad because the selection of a known material based on its suitability for its intended use is held to be obvious (MPEP 2144.07).

Referring to claims 13 and 19, the combination of Kim et al and Yoshioka teaches using a barrier layer. The combination of Kim et al and Yoshioka does not teach a diffusion barrier includes Ta or Tan. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim et al with Admission diffusion barrier of Ta or TaN to prevent diffusion between copper and aluminum, which is detrimental to resistivity (page 2 of Admission).

Referring to claim 18, the combination of Kim et al, Yoshioka and Admission teaches a copper metal line (Admission pg 3 and '826 col 2, ln 5-10), an insulating layer 53 formed over the circuit 52, this reads on applicant's dielectric, a diffusion barrier (Admission page 2 and '136 col 3, ln 65 to col 4, ln 15), an aluminum interconnection which defines a binding pad over

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openings and the conductive layer ('4, ln 15-25), first area and a second area ('136 Fig 1 and '826 Fig 5).

Referring to claim 21, the combination of Kim et al, Yoshioka and Admission teaches a second insulation layer **57** ('826 col 3, ln 45-55) and a protection layer **20** ('136 col 5, ln 10-25), which reads on applicant's passivation layer.

11. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,159,826) in view of Yoshioka (US 5,357,136) and Admission (Applicant's admitted prior art), as applied to claim 18 above, and further in view of Wood et al (US 6,107,122).

The combination of Kim et al, Yoshioka and Admission teaches all of the limitations of claim 20, as discussed previously, except the bond pad with a thickness of less than about 2 microns.

In a method of making a semiconductor device, note entire reference, Wood et al teaches typical aluminum bond pads having a thickness of from 1.0 to 1.5  $\mu\text{m}$  (col 5, ln 25-26). Wood et al also teaches electrodes can comprise thin film aluminum bond pads in electrical communication with integrated circuits (col 5, ln 15-30). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Kim et al, Yoshioka and Admission by using the aluminum pad with a thickness of 1.0 to 1.5  $\mu\text{m}$  taught by Wood et al because the thickness is conventionally used in the art.

Referring to claim 5, the combination of Kim et al, Yoshioka, Admission and Wood et al teaches a bond pad thickness of 1.0-1.5  $\mu\text{m}$ . Overlapping ranges are held to be obvious (MPEP 2144.05).

***Response to Arguments***

12. Applicant's arguments with respect to claims 1-8 and 10-24 have been considered but are moot in view of the new ground(s) of rejection.

13. Applicant's argument that Kim does not teach a bond area and a probe area on a semiconductor chip is noted but is not found persuasive. The rejection has been modified to state a portion of bond pad 56a does not overlie the metal line 52a, and this portion of the bond pad reads on applicant's probe pad because the area is capable of being probed and the area is disposed over a dielectric layer and offset from the metal line, and this portion is present on the semiconductor chip after dicing. This area reads on applicant's probe pad and meets all of the claimed structural limitations and is capable of performing the claimed intended use.

***Conclusion***

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Besser et al (US 6,239,494) teaches a diffusion barrier comprising Ti, Ta, W, an alloy thereof or a nitride (col 4, ln 5-25) and an inter-dielectric layer comprises an oxide or a nitride (col 4, ln 60-67).

Chevallier (US 6,140,665) teaches a bonding mask and a probe make are separate (col 5, ln 45-600).

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Sugasawara (US 5,936,876) teaches forming openings in a passivation layer to expose a probe pad (col 7, ln 1-25) and the probe pad is not connected to the bond pad (claim 1).

Ishikawa et al (JP 03-1516510 teaches a probe region and a bond pad region and the two part pad prevents damage to a wire bonding part (Abstract).

Buynoski (US 4,761,386) teaches a passivation layer (col 3, ln 5-25), probes contacting the bonding pads and bonding wire to the pads (col 4, ln 1-15).

Bell (US 6,429,675) teaches a first area for a bond pad and second area for a probe formed simultaneously (col 4, ln 10-30).

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J. Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Duane Smith can be reached on 571-272-1166. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew J Song  
Examiner  
Art Unit 1722

MJS  
December 8, 2005



ROBERT KUNEMUND  
PRIMARY EXAMINER